Serial No.: 09/539,405
Examiner: Kading, Joshua A.

REMARKS/ARGUMENTS

Claims 1 and 3-9 remain in this application.

Claims 1 and 3-5 have been rejected under 35 USC 102 (b) as anticipated by the US patent to Katzman et al. (4,228,496). Claim 9 has been rejected under 35 USC 103(a) as being unpatentable over Katzman. Claims 6-8 have been rejected under 35 USC 103(a) as being unpatentable over Katzman et al. in view of Diaz (U.S. 5,526,344).

Both Katzman and Diaz are systems with a bus architecture. The Examiner has likened memory 107 in processor module 33 on the bus of Katzman to the "lower level distribution module" of Applicant's claim and has compared bus clock generator 91 within the Y bus controller 37 of Katzman to Applicant's "timing generator". In Diaz, the bus time slot allocations of Fig.5b are likened to Applicant's multi-frame feedback signal.

Claim 1 has been amended to clarify that the elements of the claim are connected differently and interact differently than the structures of Katzman and Diaz to which the Examiner has called attention. For example, it is specified that the "lower level distribution module, at a control level hierarchically above the bus control modules, and coupled to the bus control modules separately from the bus." As an additional example, it is recited, "the lower level distribution module being coupled between the timing generator and the bus control modules." And further in claims 3 and 5, there are recited the "intermediate level distribution module" and "upper level distribution module" for which there are no comparable structures contemplated by Katzman and Diaz. It is submitted that the elements and their interrelation in Applicant's amended claims cannot be found in either of the cited references.

The present invention is an altogether different structure from the bus architectures of Katzman and Diaz. The system described and claimed in the present application is a hierarchical control system capable of spreading control down through the control layers and potentially to larger numbers of elements at each level. In addition, there has been conceived a multi-frame format for efficiently communicating feedback back up the control chain to the top level elements. This is not the same environment as communication between elements sharing a

common bus, wherein the basic problem is minimizing message collisions, and a solution is the allocation of bus time slots as shown in Diaz.

It is submitted that the bus systems of Katzman and Diaz do not contemplate the system, interactions, or problem solved by Applicant, or least of all, suggest any solution to the problem. Because the references are dealing with different architectures, different interactions, and different problem sets, it is respectfully submitted that claims 1 and 3-9 as amended are not anticipated by or obvious in view of Katzman, or obvious in view of Katzman considered with Diaz.

It is believed that the foregoing amendment places the Application in condition for allowance; therefore, Applicant respectfully requests withdrawal of the Examiner's rejection of claims 1 and 3-9, and allowance of same. Should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned to expeditiously resolve any outstanding issues.

The Examiner is hereby authorized to charge any necessary fees associated with this response and/or credit any overpayments to Deposit Account 50-0838.

Respectfully submitted,

ALCATEL

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